What is claimed is:

1. A method for power management of a processor comprising:

monitoring a processor utilization;

switching from a first power state to a second power state of the processor based at least in part on the processor utilization; and

switching from a first frequency for the first power state to a second frequency for the second power state within a single clock cycle.

2. The method of claim 1 wherein the first power state consumes less power than the second power state.

3. The method of claim 1 wherein switching from the first power state to the second power state is based on a higher level of processor utilization.

4. The method of claim 1 wherein switching from a first frequency for the first power state to a second frequency for the second power state within a single clock cycle comprises receiving a timing waveform from a dual phase locked loop circuit.

5. A method for supporting at least a first and second power state comprising:

generating a first Phase Locked Loop(PLL) clock for a first power state;

generating a second Phase Locked Loop clock for a second power state; and

adjusting a voltage and a frequency of a processor based at least in part on the first or second power state.

6. The method of claim 5 further comprising changing a frequency of the first Phase Locked Loop clock within a single clock cycle based on a processor utilization and changing a frequency of the second Phase Locked Loop clock after a completion of a PLL relock.

7. A method for power management of a processor comprising:

monitoring a processor utilization with a digital sensor;

switching from a first power state to a second power state of the processor based at least in part on the processor utilization; and

switching from a first frequency for the first power state to a second frequency for the second power state within a single clock cycle.

8. The method of claim 7 wherein the first power state consumes less power than the second power state.

9. The method of claim 7 wherein switching from the first power state to the second power state is based on a higher level of processor utilization.

10. The method of claim 7 wherein switching from a first frequency for the first power

state to a second frequency for the second power state within a single clock cycle comprises receiving a timing waveform from a dual phase locked loop circuit.

11. A method for supervising power consumption of a processor comprising:

setting an operating point of a frequency and a voltage for the processor;

monitoring an activity level of the processor;

adjusting a frequency of either a first or second Phase Locked Loop clock based on the activity level of the processor.

12. The method of claim 11 further comprising gating at least one clock to the processor to control power delivery of a functional unit of the processor.

13. A method for supervising power consumption of a processor comprising:

setting an operating point of a frequency and a voltage for the processor;

operating the processor in a first power state;

monitoring an activity level of the processor;

transitioning the processor to a second power state when the processor's activity

level has increased, wherein the processor operating in the second power state consumes more power than when the processors operates in the first power state.

14. The method of claim 13 further comprising gating at least one clock to the processor to control power delivery of a functional unit of the processor.

15. An system comprising:

an execution pipeline;

a digital throttle to estimate a power state, responsive to activity of the execution pipeline;

a logic to change a frequency of a first Phase Locked Loop clock within a single clock cycle based on the power state.

16. The system of claim 15 wherein the digital throttle comprises an activity monitor to provide an activity level response to activity states of units of the execution pipeline.